LISTING OF CLAIMS:

The following listing of claims replaces all previous versions and listings of claims in the present application.

1. (Currently amended) An encoder output divider configured to divide an encoded signal comprising:

a timer configured to measure a first ~~timing cycle~~period of the encoded signal~~, the encoded signal having a first period based on the measured first timing cycle~~; and

a divider coupled to the timer and configured to generate a first divided encoded signal ~~according to~~having a second period, the second period related to the first period by a multiplication factor of 1/n, where n includes an integer having a value of 2 or more.

2. (Currently amended) An encoder output divider according to claim 1, further comprising:

a calculator coupled to the divider and the timer and configured to calculate ~~the calculated~~a value based on the measured first ~~timing cycle~~period; and

an output selector coupled to the calculator, the divider and the timer and configured such that when the calculated value is within a designated range, the first divided encoded signal is selected for output, and when the calculated value is outside the designated range, the encoded signal is selected for output.

3. (Currently amended) An encoder output divider according to claim 2, wherein:

the calculated value includes a rotational speed associated with a resolver; and

the output selector is configured such that when the calculated rotational speed is within a designated range of rotational speeds, the first divided encoded signal is selected for output, and when the calculated rotational speed is outside the designated range of rotational speeds, the encoded signal is selected for output.

4. (Original) An encoder output divider according to claim 3, wherein the designated range of rotational speeds includes speeds from 400 rpm to 1200 rpm.

5. (Currently amended) A resolver/digital (R/D) converter configured to find an angle of a rotor axis of a resolver based on a sine wave output and a cosine wave output of the resolver, the R/D converter comprising:

a converter configured to convert the sine wave output and cosine wave output of the resolver into ~~a first encoded signal and a second~~ an encoded signal;

a timer coupled to the converter and configured to measure a ~~cycle~~ first period of ~~one of the first encoded signal and~~ the ~~second~~ encoded signal~~, the measured cycle corresponding to a first period associated with the one of the first encoded signal and the second encoded signal~~; and

a signal generator coupled to the converter and the timer and configured to generate a divided encoded signal having a second period, the second period related to the first period by a multiplication factor of 1/n, where n includes an integer having a value of 2 or more.

6. (Currently amended) An R/D converter according to claim 5, further comprising:

a calculator coupled to the signal generator, the converter, and the timer, the calculator configured to calculate the rotational speed of the resolver based on the measured ~~cycle~~first period of the ~~one~~encoded signal; and

an output selector coupled to the calculator, the signal generator, the converter, and the timer, the output selector configured to select the divided encoded signal for output when the calculated rotational speed of the resolver is within a designated range, and to select the encoded signal for output when the calculated rotational speed is outside the designated range.

7. (Original) An R/D converter according to claim 6, wherein the designated range of rotational speeds includes rotational speeds from 400 rpm to 1200 rpm.

8. (Currently amended) An encoder ~~capable of generating a divided encoded signal, the encoder~~ comprising:

a converter configured to convert a sine wave signal and a cosine wave signal from a resolver into ~~a first encoded signal and a second~~ an encoded signal having a first period; and

a digital signal processor (DSP) coupled to the converter, the DSP configured to:

measure [a]the first ~~cycle~~ period of ~~one of~~ the ~~first~~ encoded signal ~~and the second encoded signal to determine the first period~~,

generate ~~the~~ a divided encoded signal having a second period related to the ~~determined~~measured first period by a value of 1/n where n is an integer of 2 or greater,

determine a rotational speed associated with the resolver based on the measured first ~~cycle~~ period, and

provide a selection signal such that when the rotational speed is within a designated range, the selection signal indicates that the divided encoded signal should be output, and when the rotational speed is outside the designated range, the ~~one of the first and the second~~ encoded ~~signals~~signal should be output.

9. (Currently amended) An encoder according to claim 8, wherein

the divided encoded signal includes a first divided encoded signal and a second divided encoded signal, and

the DSP is further configured to generate [a] the second divided encoded signal offset from the first divided encoded signal by ~~half~~a quarter of the ~~first cycle~~ second period and having a period equal to the second period,

the encoder further comprising:

a multiplexer coupled to the DSP and the converter, the multiplexer configured to receive the selection signal and output the first divided encoded and the second divided encoded signal when the rotational speed is within the designated range and output the first and the second encoded signals when the rotational speed is outside the designated range.

10. (New) An encoder output divider according to claim 1, wherein the divider is further configured to generate a second divided encoded signal having the second period, the second divided encoded signal being offset in time from the first divided encoded signal by a quarter of the second period.

11. (New) An encoder output divider according to claim 2, wherein:

the divider is further configured to generate a second divided encoded signal having the second period and offset in time from the first divided encoded signal by a quarter of the second period; and

the output selector is further configured such that when the calculated value is within the designated range, the first divided encoded signal and the second divided encoded signal are selected for output, and when the calculated value is outside the designated range, the first encoded signal and the second encoded signal are selected for output.

12. (New) A resolver/digital (R/D) converter according to claim 6, wherein:

the encoded signal includes a first encoded signal and a second encoded signal each having the first period;

the divided encoded signal includes a first divided encoded signal and a second divided encoded signal each having the second period;

the signal generator is further configured to generate the second divided encoded signal offset in time from the first divided encoded signal by a quarter of the second period; and

the output selector is further configured to select the first divided encoded signal and the second divided encoded signal for output when the calculated rotational speed of the resolver is within a designated range, and to select the first encoded signal and the second encoded signal for output when the calculated rotational speed is outside the designated range.